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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

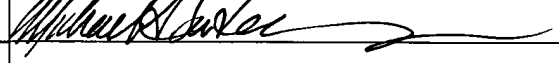
Application Number	09/053,040
Filing Dat	April 1, 1998
First Named Inventor	Isao KUDO
Group Art Unit	2876
Examiner Name	Karl D. Frech
Total Number of Pages in This Submission: 101	Attorney Docket Number: 31759-138000

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) ____
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) *(please identify below)*:

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Michael A. Sartori, Ph.D. - Reg. No. 41,289 Venable LLP P.O. Box 34385 Washington, D.C. 20043-9998	26694 PATENT TRADEMARK OFFICE
Signature		
Date	February 12, 2004	

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AF/2876

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FEE TRANSMITTAL for FY 2004

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 330

Complete if Known	
Application Number	09/053,040
Filing Date	April 1, 1998
First Named Inventor	Isao KUDO
Examiner Name	Karl D. Frech
Group / Art Unit	2876
Attorney Docket No.	31759-138000

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 22-0261

Deposit Account Name:

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☒ Payment Enclosed:

☒ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	770	2001	385	Utility filing fee	
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filling fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims		- ** =	0	X		=	0
Independent Claims		- ** =	0	X		=	0
Multiple Dependent				X		=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2204	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2215	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2010	2255	1005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	330
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,330	2453	665	Petition to revive – unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	25403	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1808	180	1808	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
				Other fee (specify) ____	

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 330

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Michael A. Sartori, Ph.D.	Registration No. Attorney/Agent	41,289	Telephone	202.344.4004
Signature				Date	February 12, 2004

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PC Docs No. 522328

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: **Isao KUDO**	Art Unit: 2876
Application No. 09/053,040	Examiner: Karl D. FRECH
Filed: April 1, 1998	Atty. Docket No. 31759-138000
Confirmation No.: 9807	
For: SEMICONDUCTOR DEVICE AND AN INFORMATION MANAGEMENT SYSTEM THEREFOR	Customer No. 26694

BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the final Office Action dated July 16, 2003.

I. Real Party in Interest

The real party in interest is Oki Electric Industry Co., Ltd. of 7-12, Toranomon 1-chome, Minato-ku, Tokyo, Japan, by virtue of an Assignment recorded on April 1, 1998 at Reel 9087, Frame 0410.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 1-22 stand finally rejected. The final rejection of claims 1-22 is appealed. No claims have been allowed.

IV. Status of Amendments

In response to the Final Office Action of July 16, 2003, Applicant filed an Amendment After Final on October 14, 2003. The Amendment requested entry of amendments to claims 1 and 11 and presented arguments for allowance of the application. An Advisory Action mailed November 20, 2003 stated that upon the filing of an appeal, the amendments to claims 1 and 11 would be entered. Because a Notice of Appeal was filed on December 16, 2003, it is assumed that the Amendment of October 14, 2003 has been entered. These changes to claims 1 and 11 are reflected in the attached Appendix.

V. Summary of the Invention

The present invention relates to a semiconductor device and an information management system for the semiconductor device that utilizes two-dimensional code patterns to efficiently

and accurately manage information about the production process for manufacturing the semiconductor device.

During the manufacturing of semiconductor devices, a large number of complicated processes must be implemented to complete the semiconductor device. Because of these complicated processes, the manufacturing of semiconductor devices requires accurate information management with respect to information on the semiconductor product during the individual processes. Historically, semiconductor devices have been mass produced in lot units, with each lot being processed under the same conditions. Recently, however, the market demand for different types of semiconductor devices produced in small quantities has increased. Accurate information management becomes even more crucial when one wafer contains a plurality of types of semiconductor devices. Specification, page 2, lines 3-29.

Conventionally, the physical distribution of semiconductor devices throughout various processes is managed by marking identification (ID) information, such as, for example, numerals and alphabetical characters, on the surface of the semiconductor chip on the wafer or on a semiconductor package that is sealed with resin. Using such a system, there is a limit to the quantity of information to be recorded and recognition of the characters during processing is difficult. Specification, page 2, line 36 to page 3 line 9.

Conventional solutions also utilize one-dimensional barcode patterns in the inter-process physical distribution of semiconductor devices. Similar to the alphanumeric characters, there is a limit to the quantity of information that can be recorded in a one-dimensional barcode pattern per

unit area. Because the area occupied by the one-dimensional barcode pattern must increase for a larger quantity of information to be carried, information management using one-dimensional barcode patterns becomes an insufficient solution. Specification, page 3, lines 12-26.

The present invention provides a two-dimensional code pattern in which specific information can be recorded by coloring the squares of a grid to form blocks that extend in two dimensions in conformance with predetermined rules. For example, referring to Figure 1, squares 11, can be colored to form code pattern 10. Specification, page 11, lines 1-5. This code pattern 10 advantageously stores more information per unit area than is possible with conventional one-dimensional patterns and can be identified through optical recognition without error.

The above and other advantages are achievable utilizing a semiconductor device as recited, for example, in independent claim 1 and shown Figures 1, 3, and 5. According to an exemplary embodiment of the invention, a semiconductor device may have at least one semiconductor chip 51 manufactured from a wafer 50, as is shown in Figure 5, for example. The semiconductor chip may have a two-dimensional code pattern 10 for information management provided directly on a surface of the at least one semiconductor chip, as shown in Figure 3, for example. See, e.g., Specification, page 13, lines 7-19. The two-dimensional code pattern may be provided on the surface of the chip 51 by projection and exposure with the pattern representing chip identification (ID) information. See, e.g., Specification, page 13, line 20 to page 14, line 5. The two-dimensional code pattern may include a plurality of square blocks 11 arranged in a

matrix in a predetermined two-dimensional region, as is shown in Figure 1, for example.

In a further exemplary embodiment of the invention, as recited in dependent claim 3 and shown in Figure 4, for example, the chip ID information may be projected and exposed using a liquid crystal mask 40 that is capable of changing a light transmitting pattern for each exposure. See, e.g., Specification, page 13, line 20 to page 14, line 31.

Further advantages are achievable utilizing a semiconductor device as recited, for example, in independent claim 4 and shown Figures 1 and 9. According to an exemplary embodiment of the invention, a semiconductor device may be manufactured using a lead frame 93, with the lead frame 93 having a two-dimensional code pattern 91 for information management provided on the lead frame 93 to which semiconductor chips 92, are bonded. The pattern 91 may be directly applied to a peripheral surface of the lead frame 93. The pattern may represent frame ID information and include a plurality of square blocks 11 arranged in a grid in a predetermined two-dimensional region. See, e.g., Specification, page 17, lines 5-11.

Independent claim 7 contains similar recitations as independent claim 1 and further recites that the semiconductor chip may be sealed by a resin. See, e.g., Specification, page 23, lines 12-17

Still a further exemplary embodiment of the invention may include an information management system for semiconductor devices as recited in independent claim 11 and shown in Figures 7 and 10, for example. In such a system, the semiconductor devices may have at least one semiconductor chip that implements management of information related to the

semiconductor devices separately for individual semiconductor devices. The information management system may include a read device, such as, for example, image recognition apparatus 107, that reads chip ID information. The chip ID information may be provided directly on the surface of the semiconductor chip by projection and exposure as a two-dimensional barcode pattern 10, as is shown in Figure 1, for example. The two-dimensional barcode pattern 10 may include a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. The information management system may also include a management unit, such as, e.g., data server 74 and database 75 in Figure 7, that registers the chip ID information and manages individual semiconductor manufacturing processes based on the registered chip ID information. See, e.g., Specification, page 15, lines 18-36.

In a further exemplary embodiment of the invention, as recited in dependent claim 12 and shown in Figure 6, for example, chip ID information may correspond to mapping data obtained during a probing process. See, e.g., Specification, page 15, lines 9-17.

Still further advantages of the invention are achievable utilizing an information management system for semiconductor devices manufactured using a lead frame as recited in independent claim 14 and shown in Figures 1, 7, 9 and 10, for example. Such a system may manage information related to said semiconductor devices separately for individual semiconductor devices. The system may include a read device, such as, e.g., image recognition apparatus 107, that reads frame ID information that is provided directly on a peripheral surface of a lead frame 93 as a two dimensional code pattern 91 for information management. The two-

dimensional code pattern 91 may include a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. The information management system may also include a management unit, such as, e.g., data server 74 and database 75, that registers the frame ID information and manages individual semiconductor manufacturing processes based on the registered frame ID information. See, e.g., Specification, page 17, line 12 to page 18, line19.

Independent claim 16 contains similar recitations as independent claim 14 and recites that the read device reads product ID information and the management unit registers the product ID information and manages individual semiconductor manufacturing processes based on the registered product ID information. See, e.g., Specification, page 26, line 29 to page 28, line 21.

In a further exemplary embodiment of the invention, as recited in dependent claim 21, for example, the two-dimensional code pattern may be formed on the semiconductor chip by photolithography. See, e.g., Specification, page 13, lines 13-20.

VI. Issues

The single issue is:

1. Whether the Examiner erred in rejecting claims 1-22 under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 5,118,369 to Shamir ("the Shamir patent") in view of U.S. Patent No. 5,659,167 to Wang et al. ("the Wang patent") and U.S. Patent No. 6,179,207 to Bossen et al ("the Bossen patent").

VII. Grouping of Claims

The claims are grouped into six groups as follows:

1. Claims 1-3 and 21 stand or fall together;

2. Claims 4-6 stand or fall together;

3. Claims 7-10 and 22 stand or fall together;

4. Claims 11-13 stand or fall together;

5. Claims 14 and 15 stand or fall together; and

6. Claims 16-20 stand or fall together.

VIII. Argument

Claims 1-22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,118,369 to Shamir in view of U.S. Patent No. 5,659,167 to Wang et al. and U.S. Patent No. 6,179,207 to Bossen et al. The cited references do not render the present invention obvious, because, among other things, they do not teach or suggest the use of a two-dimensional code that is located directly on the surface of an individual device, there is no teaching or suggestion or motive to combine the references, and combining the references in the manner suggested by the Examiner would not result in the invention as recited in the claims.

1. Claims 1-3 and 21 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Independent claim 1 recites a two-dimensional code pattern for information management provided directly on the surface of a semiconductor chip. Referring to Figures 1 and 3, for example, an embodiment of a semiconductor device as recited in claim 1 comprises at least one semiconductor chip 31-1 manufactured from a wafer (as shown in Figure 5). The at least one semiconductor chip 31-1 includes a two dimensional code pattern 10 for information management provided directly on a surface of the at least one semiconductor chip by projection and exposure. The two-dimensional pattern 10 represents chip identification (ID) information and is comprised of a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. The placing of the pattern 10 directly on the surface of at least one semiconductor chip facilitates information management at the level of the individual chips using the chip ID information provided on the chip, even when, for example, many chips are arrayed on a wafer (as shown in Figure 5).

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the

semiconductor substrate surface. Combining the three references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following four reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action. The Shamir patent discloses an arrangement wherein a label containing identifying information in the form of a conventional single dimensional bar code is placed on the device. In particular, the Shamir patent shows, referring to Figure 8, a micro label 46 having a bar code affixed to the top surface 42 of an individual die 44 as shown in Figures 1 and 2, or a micro label 122 having a bar code provided on the top surface 124 of an encapsulation 126. Shamir patent, col. 11, lines 47-52. According to the Shamir patent, only a one-dimensional bar code is disclosed, as recognized by the Office Action. While the Shamir patent does recognize that it may be necessary or desirable to have more information than that which can be placed on a single micro label, the solution to this problem according to the Shamir patent is to provide a **plurality of micro labels** containing the additional information. Shamir patent, col.4, lines 29-33. There is **no** teaching or suggestion in the Shamir patent that if it is desired to provide more information than can be provided on a single micro label with a one-dimensional bar code, a two-dimensional code pattern can be applied directly to the surface of the semiconductor chip. The Shamir patent also fails to teach or suggest that a coding system to provide more information, such as a two-

dimensional bar code pattern having a plurality of blocks located in a predetermined two-dimensional region, could be placed on a **single** bar code micro label, and hence minimize the space required for the additional information. Thus, it is submitted that contrary to the position taken by the Office Action, one skilled in the art would **not** look to a teaching, such as the Wang patent in order to provide the additional information by utilizing a two-dimensional bar code or matrix code arrangement because the Shamir patent teaches away from such a combination by urging the use of multiple one-dimensional bar codes. Thus, claim 1 is allowable for a first reason.

Second, the Shamir patent and the Wang patent fail to teach a code pattern provided directly on the surface of a chip. As pointed out above, claim 1 recites that the two-dimensional code pattern is directly provided on a surface of the chip. This recitation is contrary to the teachings of the Shamir patent, which teaches **all** of the coded information is applied **indirectly**, i.e., via micro label. Shamir patent, col. 9, lines 29-34. There is no teaching or suggestion in the Shamir patent that anything other than a micro label should be used to apply the data. On the other hand, according to claim 1, a two-dimensional code pattern is provided directly on the surface of a semiconductor chip by projection and exposure. With this arrangement according to the invention, not only can a great deal of information be recorded within a very limited space on the chip, but moreover, changes and/or peeling off of the code pattern with age is reduced so that the information recorded as a two dimensional code pattern can be reliably read out and utilized. This deficiency in the Shamir patent is recognized by the Office Action.

The Wang patent, as asserted by the Office Action, however, fails to overcome this deficiency of the Shamir patent of failing to teach a two-dimensional code pattern. The Wang patent teaches in Figure 4 that a one-dimensional bar code, a two-dimensional code or a matrix code can be used as a data form 20 and illustrates a matrix code 66 and a bar code 68. However, the Wang patent only discloses that the data form 20 is **applied** to a **card** 22. Wang patent, col. 8, lines 15-16. According to the Wang patent, data form 20 is printed on card 22 via a par code printer 18. Wang patent, col. 3, lines 63-64. There is nothing in the Wang patent which teaches providing a two-dimensional code pattern on a semiconductor chip. Moreover, there is nothing in the Wang patent which teaches or suggests that a two-dimensional code pattern should be provided directly on a surface of a semiconductor chip. In summary, while the Wang patent may teach that applying data to a card is known, it does not teach or suggest providing a two-dimensional code pattern directly to a surface of a semiconductor chip. Therefore, the Wang patent does not overcome the deficiency of the Shamir patent, and claim 1 is allowable for a second reason.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action. If one were to apply the teaching of using a two-dimensional code pattern as taught by Wang et al. to increase the information content, when combined with the Shamir patent, this combination would result in a micro label containing such a two-dimensional pattern, and **not** the providing thereof directly on a surface of a semiconductor chip. In other words, in this combination, the micro label would be placed **on**

top of the surface of the semiconductor chip, and **not** provided **directly on the surface** of the semiconductor chip. The claimed invention recites a two-dimensional code pattern for information management provided directly on a surface of a semiconductor chip. The claimed invention does not recite a micro label containing a two-dimensional pattern as taught by the resulting combination of the Shamir patent and the Wang patent. Thus, claim 1 is allowable for a third reason

Fourth, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Claim 1 recites that the information is provided directly on the surface of a semiconductor chip. Claim 1 further recites that the information on the surface of the chip is provided by projection and exposure. That is, the information is provided directly on the surface of the semiconductor chip. Such is not the case according to the teachings of the cited prior art in any combination thereof. As acknowledged by the Office Action the Shamir patent and the Wang patent fail to teach this recitation. To overcome this deficiency, the Office Action relies on the Bossen patent. The Bossen patent teaches **laser etching** the surface of a semiconductor device to provide information in the form of a **one-dimensional barcode**. Bossen patent, col. 5, lines 60-64. The Bossen patent, however, does **not** teach laser etching a two-dimensional bar code **directly on** a surface. Instead, with the teachings of the Bossen patent, the information is formed **in** the device **adjacent** the outer surface. Hence, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Thus, claim 1 is allowable for a fourth reason.

Accordingly, for the above stated reasons, it is submitted that claim 1 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 2-3 and 21 depend from claim 1 and are allowable as being dependent from an allowable claim.

2. Claims 4-6 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Independent claim 4 recites a two-dimensional code pattern for information management provided directly on the surface of a lead frame. Referring to Figures 1 and 9, for example, an embodiment of a semiconductor device as recited in claim 4 comprises a semiconductor device manufactured using a lead frame 93, with the lead frame 93 having a two-dimensional code pattern 91 for information management provided on the lead frame 93 to which semiconductor chips 92 are bonded. The pattern 91 may be directly applied to a peripheral surface of the lead frame 93. The pattern may represent frame ID information and include a plurality of square blocks 11 arranged in a grid in a predetermined two-dimensional region. With the recited two-dimensional code pattern on a peripheral region of a lead frame, information can be easily recognized and a wiring pattern to be bonded can be easily changed during the wire bonding as described.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional

barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the three references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following five reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Claim 4 recites that the two-dimensional code pattern is directly applied to a peripheral surface of the lead frame. As discussed above for claim 1, the Bossen patent teaches **laser etching** the surface of a semiconductor device to provide information in the form of a **one-dimensional barcode**. Bossen patent, col. 5, lines 60-64. The Bossen patent, however, does **not**

teach laser etching a two-dimensional bar code **directly on** a surface. Instead, with the teachings of the Bossen patent, the information is formed **in** the device **adjacent** the outer surface. Hence, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Thus, claim 4 is allowable for at least a fourth reason.

Fifth, none of the three documents cited to reject claim 4 teach that a that the peripheral surface to which a two-dimensional pattern is directly applied is a peripheral surface of a lead frame. The Office Action fails to address the recitation of a lead frame. Further, there is no teaching or suggestion in any of the cited patents that would make it obvious to apply two-dimensional code patterns to a peripheral surface of a lead frame.

Thus, for at least the above five reasons, claim 4 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 5-6 depend on claim 4 and are allowable as being dependent from an allowable claim.

3. Claims 7-10 and 22 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 7 recites similar recitations as independent claim 1, and further recites that the semiconductor chip may be sealed by a resin. Specifically, claim 7 recites a two-dimensional code pattern for information management provided directly on an outer surface of a semiconductor chip sealed by resin.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the three references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following five reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Claim 7 recites that the two-dimensional code pattern is provided directly on an

outer surface of semiconductor chip sealed by resin. As discussed above for claim 1, the Bossen patent teaches **laser etching** the surface of a semiconductor device to provide information in the form of a **one-dimensional barcode**. Bossen patent, col. 5, lines 60-64. The Bossen patent, however, does **not** teach laser etching a two-dimensional bar code **directly on** a surface. Instead, with the teachings of the Bossen patent, the information is formed **in** the device **adjacent** the outer surface. Hence, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Thus, claim 7 is allowable for at least a fourth reason.

Fifth, none of the three documents cited to reject claim 7 teach that a that the peripheral surface to which a two-dimensional pattern is applied is an outer surface of a semiconductor chip sealed by resin. The Office Action fails to address the recitation of a resin-sealed chip. Further, there is no teaching or suggestion in any of the cited patents that would make it obvious to apply two-dimensional patterns to the outer surface of a semiconductor chip sealed by resin.

Thus, for at least the above five reasons, claim 7 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 8-10 and 22 depend from claim 7 and are allowable as being dependent from an allowable claim.

4. Claims 11-13 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 11 recites an information management system for semiconductor devices. In such a system, the semiconductor devices may have at least one semiconductor chip that implements

management of information related to the semiconductor devices separately for individual semiconductor devices. Referring to Figure 10, for example, the information management system may include a read device, such as, image recognition apparatus 107, that reads chip ID information. Referring to Figure 11, for example, the chip ID information may be provided directly on the surface of the semiconductor chip by projection and exposure as a two-dimensional barcode pattern 10, which may include a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. Referring to Figure 7, for example, the information management system may also include a management unit, such as, data server 74 and database 75, that registers the chip ID information and manages individual semiconductor manufacturing processes based on the registered chip ID information.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by

the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following four reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent fails to teach or suggest all of the recitations of claim 11. Claim11 is directed to an information management system, which requires a read device that reads chip ID information provided directly on a surface of a chip as a two-dimensional code pattern, and a management unit that reads the chip ID information and manages individual semiconductor manufacturing processes. None of the cited references to reject claim 11 teach components of an information management system, including a read device and a management unit. It is noted that the Office Action has failed to comment on the recitation of these features and failed to point out where they are found in the references in any of the three patents. Hence, claim 11 is allowable for a fourth reason.

Thus, for at least the above four reasons, claim 11 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 12-13 depend from claim 11 and are allowable as being dependent from an allowable claim.

5. Claims 14 and 15 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 14 an information management system for semiconductor devices. Such a system may manage information related to said semiconductor devices separately for individual semiconductor devices. Referring to Figures 9 and 10, for example, the system may include a read device, such as, e.g., image recognition apparatus 107, that reads frame ID information that is provided directly on a peripheral surface of a lead frame 93 as a two dimensional code pattern 91 for information management. The two-dimensional code pattern 91 may include a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. Referring to Figure 7, for example, the information management system may also include a management unit, such as, e.g., data server 74 and database 75, that registers the frame ID information and manages individual semiconductor manufacturing processes based on the registered frame ID information.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has

interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following five reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent fails to teach or suggest providing a two-dimensional code pattern directly on a peripheral surface of a lead frame, as similarly discussed above for claim 4.

Fifth, the three-way combination of the Shamir patent, the Wang patent and the Bossen patent fails to teach or suggest an information management system which requires a read device that reads frame ID information provided on a lead frame as a two-dimensional code pattern, and a management unit that reads the frame ID information and manages individual semiconductor manufacturing processes, as similarly discussed for claim 11

Thus, for at least the above five reasons, claim 14 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 15 depends from 14 and is allowable dependent from an allowable claim.

6. Claims 16-20 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 16 is similar to claim 14 and additionally recites that the read device reads product ID information and the management unit registers the product ID information and manages individual semiconductor manufacturing processes based on the registered product ID information.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by

the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following five reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent fails to teach or suggest providing a two-dimensional code pattern directly on an outer surface of a resin sealed semiconductor chip, as similarly discussed above for claim 7.

Fifth, the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent fail to teach or suggest an information management system which requires a read device that reads product ID information provided as a two-dimensional code pattern on an outer surface of a resin sealed semiconductor chip, and a management unit that registers the product ID information and manages a product shipping process, as similarly discussed above for claim 11.

Thus, for at least the above five reasons, claim 16 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 17-20 depend from claim 16 and are allowable as being dependent from an allowable claim.

In view of the foregoing, it is submitted that the rejection of claims 1-22 should not be sustained, and a decision to that effect is respectfully requested.

A check in the amount of $330.00 is enclosed for the submission of this Appeal Brief. However, if any additional fee is due, the Commissioner is hereby authorized to charge and/or credit any fees to Deposit Account No. 22-0261.

Respectfully submitted,

Date: February 17, 2004

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X. APPENDIX

1. *(Previously Presented)* A semiconductor device having at least one semiconductor chip manufactured from a wafer, said semiconductor chip having a two-dimensional code pattern for information management provided directly on a surface of said at least one semiconductor chip by projection and exposure with the pattern representing chip ID information, and said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

2. *(Original)* A semiconductor device according to claim 1, wherein:

said chip ID information includes chip information inherent to each chip.

3. *(Original)* A semiconductor device according to claim 1, wherein:

said chip ID information is projected and exposed using a liquid crystal mask that is capable of changing a light transmitting pattern for each exposure.

4. *(Previously Presented)* A semiconductor device manufactured using a lead frame, with the lead frame having a two-dimensional code pattern for information management provided on said lead frame to which semiconductor chips are bonded, with the pattern being

directly applied to a peripheral surface of the lead frame and representing frame ID information, and said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a grid in a predetermined two-dimensional region.

5. *(Original)* A semiconductor device according to claim 4, wherein:

said frame ID information includes chip positional information corresponding to chips within said frame.

6. *(Previously Presented)* A semiconductor device according to claim 4, wherein:

said frame ID information is made to correspond to chip ID information provided as a two-dimensional barcode pattern for information management for each chip.

7. *(Previously Presented)* A semiconductor device having at least one semiconductor chip sealed by resin, and having a two-dimensional code pattern for information management provided directly on an outer surface of said resin and representing product ID information, and said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

8. *(Original)* A semiconductor device according to claim 7, wherein:

said product ID information includes additional information corresponding to individual chips that are resin-sealed.

9. *(Previously Presented)* A semiconductor device according to claim 7, wherein:

said product ID information corresponds to chip ID information provided as a two-dimensional barcode pattern for information management for each chip.

10. *(Previously Presented)* A semiconductor device according to claim 7, wherein:

said product ID information corresponds to frame ID information provided as a two-dimensional barcode pattern for information management on a lead frame to which semiconductor chips are bonded.

11. *(Previously Presented)* An information management system for semiconductor devices, having at least one semiconductor chip that implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads chip ID information, said chip ID information is provided

directly on a surface of said semiconductor chip by projection and exposure as a two-dimensional barcode pattern for information management for each chip, said two-dimensional barcode pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said chip ID information thus read and manages individual semiconductor manufacturing processes based upon said chip ID information thus registered.

12. *(Previously Presented)* An information management system for semiconductor devices according to claim 11, wherein:

said chip ID information is made to correspond to mapping data obtained during a probing process.

13. *(Original)* An information management system for semiconductor devices according to claim 11, wherein:

said chip ID *information* is projected and exposed using a liquid crystal mask that is capable of changing a light transmitting pattern for each exposure.

14. *(Previously Presented)* An information management system for semiconductor device manufactured using a lead frame, which system implements management of information

related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads frame ID information, said frame ID information is provided directly on a peripheral surface of said lead frame as a two-dimensional code pattern for information management, said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said frame ID information thus read and manages individual semiconductor manufacturing processes based upon said frame ID information thus registered.

15. *(Previously Presented)* An information management system for semiconductor devices according to claim 14, wherein:

said frame ID information corresponds to chip ID information provided as a two-dimensional barcode pattern for information management for each chip.

16. *(Previously Presented)* An information management system for semiconductor devices having semiconductor chips sealed by resin, which system implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads product ID information, said product ID information is

provided as a two-dimensional code pattern for information management directly on an outer surface of said resin, said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said product ID information and manages a product shipping process based upon said product ID information thus registered.

17. *(Previously Presented)* An information management system for semiconductor devices according to claim 16, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional barcode pattern for information management for each chip.

18. *(Previously Presented)* A semiconductor device according to claim 16, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional barcode pattern for information management on a lead frame to which semiconductor chips are bonded.

19. *(Previously Presented)* An information management system for semiconductor devices according to claim 16, wherein:

said product ID information that is registered corresponds to manufacturing

process history information corresponding to each chip.

20. *(Previously Presented)* An information management system for semiconductor devices according to claim 16, wherein:

said product ID information that is registered corresponds to claim information regarding claims made in the field after product shipment.

21. *(Previously Presented)* A semiconductor device according to claim 1, wherein said two-dimensional code pattern is formed on said semiconductor chip by photolithography.

22. *(Previously Presented)* A semiconductor device according to claim 7, wherein the blocks of two-dimensional code are formed by laser printing directly on the outer surface of the resin.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: **Isao KUDO**	Art Unit: 2876
Application No. 09/053,040	Examiner: Karl D. FRECH
Filed: April 1, 1998	Atty. Docket No. 31759-138000
Confirmation No.: 9807	
For: SEMICONDUCTOR DEVICE AND AN INFORMATION MANAGEMENT SYSTEM THEREFOR	Customer No. 26694

BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the final Office Action dated July 16, 2003.

I. Real Party in Interest

The real party in interest is Oki Electric Industry Co., Ltd. of 7-12, Toranomon 1-chome, Minato-ku, Tokyo, Japan, by virtue of an Assignment recorded on April 1, 1998 at Reel 9087, Frame 0410.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 1-22 stand finally rejected. The final rejection of claims 1-22 is appealed. No claims have been allowed.

IV. Status of Amendments

In response to the Final Office Action of July 16, 2003, Applicant filed an Amendment After Final on October 14, 2003. The Amendment requested entry of amendments to claims 1 and 11 and presented arguments for allowance of the application. An Advisory Action mailed November 20, 2003 stated that upon the filing of an appeal, the amendments to claims 1 and 11 would be entered. Because a Notice of Appeal was filed on December 16, 2003, it is assumed that the Amendment of October 14, 2003 has been entered. These changes to claims 1 and 11 are reflected in the attached Appendix.

V. Summary of the Invention

The present invention relates to a semiconductor device and an information management system for the semiconductor device that utilizes two-dimensional code patterns to efficiently

and accurately manage information about the production process for manufacturing the semiconductor device.

During the manufacturing of semiconductor devices, a large number of complicated processes must be implemented to complete the semiconductor device. Because of these complicated processes, the manufacturing of semiconductor devices requires accurate information management with respect to information on the semiconductor product during the individual processes. Historically, semiconductor devices have been mass produced in lot units, with each lot being processed under the same conditions. Recently, however, the market demand for different types of semiconductor devices produced in small quantities has increased. Accurate information management becomes even more crucial when one wafer contains a plurality of types of semiconductor devices. Specification, page 2, lines 3-29.

Conventionally, the physical distribution of semiconductor devices throughout various processes is managed by marking identification (ID) information, such as, for example, numerals and alphabetical characters, on the surface of the semiconductor chip on the wafer or on a semiconductor package that is sealed with resin. Using such a system, there is a limit to the quantity of information to be recorded and recognition of the characters during processing is difficult. Specification, page 2, line 36 to page 3 line 9.

Conventional solutions also utilize one-dimensional barcode patterns in the inter-process physical distribution of semiconductor devices. Similar to the alphanumeric characters, there is a limit to the quantity of information that can be recorded in a one-dimensional barcode pattern per

unit area. Because the area occupied by the one-dimensional barcode pattern must increase for a larger quantity of information to be carried, information management using one-dimensional barcode patterns becomes an insufficient solution. Specification, page 3, lines 12-26.

The present invention provides a two-dimensional code pattern in which specific information can be recorded by coloring the squares of a grid to form blocks that extend in two dimensions in conformance with predetermined rules. For example, referring to Figure 1, squares 11, can be colored to form code pattern 10. Specification, page 11, lines 1-5. This code pattern 10 advantageously stores more information per unit area than is possible with conventional one-dimensional patterns and can be identified through optical recognition without error.

The above and other advantages are achievable utilizing a semiconductor device as recited, for example, in independent claim 1 and shown Figures 1, 3, and 5. According to an exemplary embodiment of the invention, a semiconductor device may have at least one semiconductor chip 51 manufactured from a wafer 50, as is shown in Figure 5, for example. The semiconductor chip may have a two-dimensional code pattern 10 for information management provided directly on a surface of the at least one semiconductor chip, as shown in Figure 3, for example. See, e.g., Specification, page 13, lines 7-19. The two-dimensional code pattern may be provided on the surface of the chip 51 by projection and exposure with the pattern representing chip identification (ID) information. See, e.g., Specification, page 13, line 20 to page 14, line 5. The two-dimensional code pattern may include a plurality of square blocks 11 arranged in a

matrix in a predetermined two-dimensional region, as is shown in Figure 1, for example.

In a further exemplary embodiment of the invention, as recited in dependent claim 3 and shown in Figure 4, for example, the chip ID information may be projected and exposed using a liquid crystal mask 40 that is capable of changing a light transmitting pattern for each exposure. See, e.g., Specification, page 13, line 20 to page 14, line 31.

Further advantages are achievable utilizing a semiconductor device as recited, for example, in independent claim 4 and shown Figures 1 and 9. According to an exemplary embodiment of the invention, a semiconductor device may be manufactured using a lead frame 93, with the lead frame 93 having a two-dimensional code pattern 91 for information management provided on the lead frame 93 to which semiconductor chips 92, are bonded. The pattern 91 may be directly applied to a peripheral surface of the lead frame 93. The pattern may represent frame ID information and include a plurality of square blocks 11 arranged in a grid in a predetermined two-dimensional region. See, e.g., Specification, page 17, lines 5-11.

Independent claim 7 contains similar recitations as independent claim 1 and further recites that the semiconductor chip may be sealed by a resin. See, e.g., Specification, page 23, lines 12-17

Still a further exemplary embodiment of the invention may include an information management system for semiconductor devices as recited in independent claim 11 and shown in Figures 7 and 10, for example. In such a system, the semiconductor devices may have at least one semiconductor chip that implements management of information related to the

semiconductor devices separately for individual semiconductor devices. The information management system may include a read device, such as, for example, image recognition apparatus 107, that reads chip ID information. The chip ID information may be provided directly on the surface of the semiconductor chip by projection and exposure as a two-dimensional barcode pattern 10, as is shown in Figure 1, for example. The two-dimensional barcode pattern 10 may include a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. The information management system may also include a management unit, such as, e.g., data server 74 and database 75 in Figure 7, that registers the chip ID information and manages individual semiconductor manufacturing processes based on the registered chip ID information. See, e.g., Specification, page 15, lines 18-36.

In a further exemplary embodiment of the invention, as recited in dependent claim 12 and shown in Figure 6, for example, chip ID information may correspond to mapping data obtained during a probing process. See, e.g., Specification, page 15, lines 9-17.

Still further advantages of the invention are achievable utilizing an information management system for semiconductor devices manufactured using a lead frame as recited in independent claim 14 and shown in Figures 1, 7, 9 and 10, for example. Such a system may manage information related to said semiconductor devices separately for individual semiconductor devices. The system may include a read device, such as, e.g., image recognition apparatus 107, that reads frame ID information that is provided directly on a peripheral surface of a lead frame 93 as a two dimensional code pattern 91 for information management. The two-

dimensional code pattern 91 may include a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. The information management system may also include a management unit, such as, e.g., data server 74 and database 75, that registers the frame ID information and manages individual semiconductor manufacturing processes based on the registered frame ID information. See, e.g., Specification, page 17, line 12 to page 18, line19.

Independent claim 16 contains similar recitations as independent claim 14 and recites that the read device reads product ID information and the management unit registers the product ID information and manages individual semiconductor manufacturing processes based on the registered product ID information. See, e.g., Specification, page 26, line 29 to page 28, line 21.

In a further exemplary embodiment of the invention, as recited in dependent claim 21, for example, the two-dimensional code pattern may be formed on the semiconductor chip by photolithography. See, e.g., Specification, page 13, lines 13-20.

VI. Issues

The single issue is:

1. Whether the Examiner erred in rejecting claims 1-22 under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 5,118,369 to Shamir ("the Shamir patent") in view of U.S. Patent No. 5,659,167 to Wang et al. ("the Wang patent") and U.S. Patent No. 6,179,207 to Bossen et al ("the Bossen patent").

VII. Grouping of Claims

The claims are grouped into six groups as follows:

1. Claims 1-3 and 21 stand or fall together;

2. Claims 4-6 stand or fall together;

3. Claims 7-10 and 22 stand or fall together;

4. Claims 11-13 stand or fall together;

5. Claims 14 and 15 stand or fall together; and

6. Claims 16-20 stand or fall together.

VIII. Argument

Claims 1-22 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,118,369 to Shamir in view of U.S. Patent No. 5,659,167 to Wang et al. and U.S. Patent No. 6,179,207 to Bossen et al. The cited references do not render the present invention obvious, because, among other things, they do not teach or suggest the use of a two-dimensional code that is located directly on the surface of an individual device, there is no teaching or suggestion or motive to combine the references, and combining the references in the manner suggested by the Examiner would not result in the invention as recited in the claims.

1. Claims 1-3 and 21 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Independent claim 1 recites a two-dimensional code pattern for information management provided directly on the surface of a semiconductor chip. Referring to Figures 1 and 3, for example, an embodiment of a semiconductor device as recited in claim 1 comprises at least one semiconductor chip 31-1 manufactured from a wafer (as shown in Figure 5). The at least one semiconductor chip 31-1 includes a two dimensional code pattern 10 for information management provided directly on a surface of the at least one semiconductor chip by projection and exposure. The two-dimensional pattern 10 represents chip identification (ID) information and is comprised of a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. The placing of the pattern 10 directly on the surface of at least one semiconductor chip facilitates information management at the level of the individual chips using the chip ID information provided on the chip, even when, for example, many chips are arrayed on a wafer (as shown in Figure 5).

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the

semiconductor substrate surface. Combining the three references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following four reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action. The Shamir patent discloses an arrangement wherein a label containing identifying information in the form of a conventional single dimensional bar code is placed on the device. In particular, the Shamir patent shows, referring to Figure 8, a micro label 46 having a bar code affixed to the top surface 42 of an individual die 44 as shown in Figures 1 and 2, or a micro label 122 having a bar code provided on the top surface 124 of an encapsulation 126. Shamir patent, col. 11, lines 47-52. According to the Shamir patent, only a one-dimensional bar code is disclosed, as recognized by the Office Action. While the Shamir patent does recognize that it may be necessary or desirable to have more information than that which can be placed on a single micro label, the solution to this problem according to the Shamir patent is to provide a **plurality of micro labels** containing the additional information. Shamir patent, col.4, lines 29-33. There is **no** teaching or suggestion in the Shamir patent that if it is desired to provide more information than can be provided on a single micro label with a one-dimensional bar code, a two-dimensional code pattern can be applied directly to the surface of the semiconductor chip. The Shamir patent also fails to teach or suggest that a coding system to provide more information, such as a two-

dimensional bar code pattern having a plurality of blocks located in a predetermined two-dimensional region, could be placed on a **single** bar code micro label, and hence minimize the space required for the additional information. Thus, it is submitted that contrary to the position taken by the Office Action, one skilled in the art would **not** look to a teaching, such as the Wang patent in order to provide the additional information by utilizing a two-dimensional bar code or matrix code arrangement because the Shamir patent teaches away from such a combination by urging the use of multiple one-dimensional bar codes. Thus, claim 1 is allowable for a first reason.

Second, the Shamir patent and the Wang patent fail to teach a code pattern provided directly on the surface of a chip. As pointed out above, claim 1 recites that the two-dimensional code pattern is directly provided on a surface of the chip. This recitation is contrary to the teachings of the Shamir patent, which teaches **all** of the coded information is applied **indirectly**, i.e., via micro label. Shamir patent, col. 9, lines 29-34. There is no teaching or suggestion in the Shamir patent that anything other than a micro label should be used to apply the data. On the other hand, according to claim 1, a two-dimensional code pattern is provided directly on the surface of a semiconductor chip by projection and exposure. With this arrangement according to the invention, not only can a great deal of information be recorded within a very limited space on the chip, but moreover, changes and/or peeling off of the code pattern with age is reduced so that the information recorded as a two dimensional code pattern can be reliably read out and utilized. This deficiency in the Shamir patent is recognized by the Office Action.

The Wang patent, as asserted by the Office Action, however, fails to overcome this deficiency of the Shamir patent of failing to teach a two-dimensional code pattern. The Wang patent teaches in Figure 4 that a one-dimensional bar code, a two-dimensional code or a matrix code can be used as a data form 20 and illustrates a matrix code 66 and a bar code 68. However, the Wang patent only discloses that the data form 20 is **applied** to a **card** 22. Wang patent, col. 8, lines 15-16. According to the Wang patent, data form 20 is printed on card 22 via a par code printer 18. Wang patent, col. 3, lines 63-64. There is nothing in the Wang patent which teaches providing a two-dimensional code pattern on a semiconductor chip. Moreover, there is nothing in the Wang patent which teaches or suggests that a two-dimensional code pattern should be provided directly on a surface of a semiconductor chip. In summary, while the Wang patent may teach that applying data to a card is known, it does not teach or suggest providing a two-dimensional code pattern directly to a surface of a semiconductor chip. Therefore, the Wang patent does not overcome the deficiency of the Shamir patent, and claim 1 is allowable for a second reason.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action. If one were to apply the teaching of using a two-dimensional code pattern as taught by Wang et al. to increase the information content, when combined with the Shamir patent, this combination would result in a micro label containing such a two-dimensional pattern, and **not** the providing thereof directly on a surface of a semiconductor chip. In other words, in this combination, the micro label would be placed **on**

top of the surface of the semiconductor chip, and not provided directly on the surface of the semiconductor chip. The claimed invention recites a two-dimensional code pattern for information management provided directly on a surface of a semiconductor chip. The claimed invention does not recite a micro label containing a two-dimensional pattern as taught by the resulting combination of the Shamir patent and the Wang patent. Thus, claim 1 is allowable for a third reason

Fourth, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Claim 1 recites that the information is provided directly on the surface of a semiconductor chip. Claim 1 further recites that the information on the surface of the chip is provided by projection and exposure. That is, the information is provided directly on the surface of the semiconductor chip. Such is not the case according to the teachings of the cited prior art in any combination thereof. As acknowledged by the Office Action the Shamir patent and the Wang patent fail to teach this recitation. To overcome this deficiency, the Office Action relies on the Bossen patent. The Bossen patent teaches **laser etching** the surface of a semiconductor device to provide information in the form of a **one-dimensional barcode**. Bossen patent, col. 5, lines 60-64. The Bossen patent, however, does **not** teach laser etching a two-dimensional bar code **directly on** a surface. Instead, with the teachings of the Bossen patent, the information is formed **in** the device **adjacent** the outer surface. Hence, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Thus, claim 1 is allowable for a fourth reason.

Accordingly, for the above stated reasons, it is submitted that claim 1 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 2-3 and 21 depend from claim 1 and are allowable as being dependent from an allowable claim.

2. Claims 4-6 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Independent claim 4 recites a two-dimensional code pattern for information management provided directly on the surface of a lead frame. Referring to Figures 1 and 9, for example, an embodiment of a semiconductor device as recited in claim 4 comprises a semiconductor device manufactured using a lead frame 93, with the lead frame 93 having a two-dimensional code pattern 91 for information management provided on the lead frame 93 to which semiconductor chips 92 are bonded. The pattern 91 may be directly applied to a peripheral surface of the lead frame 93. The pattern may represent frame ID information and include a plurality of square blocks 11 arranged in a grid in a predetermined two-dimensional region. With the recited two-dimensional code pattern on a peripheral region of a lead frame, information can be easily recognized and a wiring pattern to be bonded can be easily changed during the wire bonding as described.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional

barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the three references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following five reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Claim 4 recites that the two-dimensional code pattern is directly applied to a peripheral surface of the lead frame. As discussed above for claim 1, the Bossen patent teaches **laser etching** the surface of a semiconductor device to provide information in the form of a **one-dimensional barcode**. Bossen patent, col. 5, lines 60-64. The Bossen patent, however, does **not**

teach laser etching a two-dimensional bar code **directly on** a surface. Instead, with the teachings of the Bossen patent, the information is formed **in** the device **adjacent** the outer surface. Hence, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Thus, claim 4 is allowable for at least a fourth reason.

Fifth, none of the three documents cited to reject claim 4 teach that a that the peripheral surface to which a two-dimensional pattern is directly applied is a peripheral surface of a lead frame. The Office Action fails to address the recitation of a lead frame. Further, there is no teaching or suggestion in any of the cited patents that would make it obvious to apply two-dimensional code patterns to a peripheral surface of a lead frame.

Thus, for at least the above five reasons, claim 4 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 5-6 depend on claim 4 and are allowable as being dependent from an allowable claim.

3. Claims 7-10 and 22 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 7 recites similar recitations as independent claim 1, and further recites that the semiconductor chip may be sealed by a resin. Specifically, claim 7 recites a two-dimensional code pattern for information management provided directly on an outer surface of a semiconductor chip sealed by resin.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the three references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following five reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Claim 7 recites that the two-dimensional code pattern is provided directly on an

outer surface of semiconductor chip sealed by resin. As discussed above for claim 1, the Bossen patent teaches **laser etching** the surface of a semiconductor device to provide information in the form of a **one-dimensional barcode**. Bossen patent, col. 5, lines 60-64. The Bossen patent, however, does **not** teach laser etching a two-dimensional bar code **directly on** a surface. Instead, with the teachings of the Bossen patent, the information is formed **in** the device **adjacent** the outer surface. Hence, the Bossen patent fails to overcome the deficiencies of the Shamir patent and the Wang patent. Thus, claim 7 is allowable for at least a fourth reason.

Fifth, none of the three documents cited to reject claim 7 teach that a that the peripheral surface to which a two-dimensional pattern is applied is an outer surface of a semiconductor chip sealed by resin. The Office Action fails to address the recitation of a resin-sealed chip. Further, there is no teaching or suggestion in any of the cited patents that would make it obvious to apply two-dimensional patterns to the outer surface of a semiconductor chip sealed by resin.

Thus, for at least the above five reasons, claim 7 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 8-10 and 22 depend from claim 7 and are allowable as being dependent from an allowable claim.

4. Claims 11-13 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 11 recites an information management system for semiconductor devices. In such a system, the semiconductor devices may have at least one semiconductor chip that implements

management of information related to the semiconductor devices separately for individual semiconductor devices. Referring to Figure 10, for example, the information management system may include a read device, such as, image recognition apparatus 107, that reads chip ID information. Referring to Figure 11, for example, the chip ID information may be provided directly on the surface of the semiconductor chip by projection and exposure as a two-dimensional barcode pattern 10, which may include a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. Referring to Figure 7, for example, the information management system may also include a management unit, such as, data server 74 and database 75, that registers the chip ID information and manages individual semiconductor manufacturing processes based on the registered chip ID information.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by

the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following four reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent fails to teach or suggest all of the recitations of claim 11. Claim11 is directed to an information management system, which requires a read device that reads chip ID information provided directly on a surface of a chip as a two-dimensional code pattern, and a management unit that reads the chip ID information and manages individual semiconductor manufacturing processes. None of the cited references to reject claim 11 teach components of an information management system, including a read device and a management unit. It is noted that the Office Action has failed to comment on the recitation of these features and failed to point out where they are found in the references in any of the three patents. Hence, claim 11 is allowable for a fourth reason.

Thus, for at least the above four reasons, claim 11 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 12-13 depend from claim 11 and are allowable as being dependent from an allowable claim.

5. Claims 14 and 15 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 14 an information management system for semiconductor devices. Such a system may manage information related to said semiconductor devices separately for individual semiconductor devices. Referring to Figures 9 and 10, for example, the system may include a read device, such as, e.g., image recognition apparatus 107, that reads frame ID information that is provided directly on a peripheral surface of a lead frame 93 as a two dimensional code pattern 91 for information management. The two-dimensional code pattern 91 may include a plurality of square blocks 11 arranged in a matrix in a predetermined two-dimensional region. Referring to Figure 7, for example, the information management system may also include a management unit, such as, e.g., data server 74 and database 75, that registers the frame ID information and manages individual semiconductor manufacturing processes based on the registered frame ID information.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has

interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following five reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent fails to teach or suggest providing a two-dimensional code pattern directly on a peripheral surface of a lead frame, as similarly discussed above for claim 4.

Fifth, the three-way combination of the Shamir patent, the Wang patent and the Bossen patent fails to teach or suggest an information management system which requires a read device that reads frame ID information provided on a lead frame as a two-dimensional code pattern, and a management unit that reads the frame ID information and manages individual semiconductor manufacturing processes, as similarly discussed for claim 11

Thus, for at least the above five reasons, claim 14 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 15 depends from 14 and is allowable dependent from an allowable claim.

6. Claims 16-20 are patentable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claim 16 is similar to claim 14 and additionally recites that the read device reads product ID information and the management unit registers the product ID information and manages individual semiconductor manufacturing processes based on the registered product ID information.

In asserting this ground of rejection, the Office Action has interpreted the Shamir patent as disclosing a wafer with a plurality of semiconductor dies having individual information regarding the particular die being placed on the respective die in the form of one dimensional barcode labels. The Office Action has interpreted the Wang patent to teach that two-dimensional barcodes are known in the art, and that the Shamir and Wang patents do not disclose that the barcodes are directly on the surfaces of a device. To overcome this deficiency, the Office has interpreted the Bossen patent as disclosing that barcodes are etched directly onto the semiconductor substrate surface. Combining the references, the Office Action asserts that it would be obvious to one skilled in the art to provide a code as taught by the Wang patent on the device as taught by the Shamir patent, and to provide the code directly on the surface as taught by

the Bossen patent. The Examiner's conclusion is respectfully traversed for at least the following five reasons.

First, the Shamir patent teaches away from the combination proposed by the Office Action for the same reasons discussed above for claim 1.

Second, the Shamir patent and the Wang patent fail to teach a code pattern directly on the surface of a chip as discussed above for claim 1.

Third, the combination of the Shamir patent and the Wang patent fails to teach the claimed invention as postulated by the Office Action and discussed above for claim 1.

Fourth, the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent fails to teach or suggest providing a two-dimensional code pattern directly on an outer surface of a resin sealed semiconductor chip, as similarly discussed above for claim 7.

Fifth, the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent fail to teach or suggest an information management system which requires a read device that reads product ID information provided as a two-dimensional code pattern on an outer surface of a resin sealed semiconductor chip, and a management unit that registers the product ID information and manages a product shipping process, as similarly discussed above for claim 11.

Thus, for at least the above five reasons, claim 16 is allowable over the three-way combination of the Shamir patent, the Wang patent, and the Bossen patent.

Claims 17-20 depend from claim 16 and are allowable as being dependent from an allowable claim.

In view of the foregoing, it is submitted that the rejection of claims 1-22 should not be sustained, and a decision to that effect is respectfully requested.

A check in the amount of $330.00 is enclosed for the submission of this Appeal Brief. However, if any additional fee is due, the Commissioner is hereby authorized to charge and/or credit any fees to Deposit Account No. 22-0261.

Respectfully submitted,

Date: February 12, 2004

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X. APPENDIX

1. *(Previously Presented)* A semiconductor device having at least one semiconductor chip manufactured from a wafer, said semiconductor chip having a two-dimensional code pattern for information management provided directly on a surface of said at least one semiconductor chip by projection and exposure with the pattern representing chip ID information, and said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

2. *(Original)* A semiconductor device according to claim 1, wherein:

said chip ID information includes chip information inherent to each chip.

3. *(Original)* A semiconductor device according to claim 1, wherein:

said chip ID information is projected and exposed using a liquid crystal mask that is capable of changing a light transmitting pattern for each exposure.

4. *(Previously Presented)* A semiconductor device manufactured using a lead frame, with the lead frame having a two-dimensional code pattern for information management provided on said lead frame to which semiconductor chips are bonded, with the pattern being

directly applied to a peripheral surface of the lead frame and representing frame ID information, and said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a grid in a predetermined two-dimensional region.

5. *(Original)* A semiconductor device according to claim 4, wherein:

said frame ID information includes chip positional information corresponding to chips within said frame.

6. *(Previously Presented)* A semiconductor device according to claim 4, wherein:

said frame ID information is made to correspond to chip ID information provided as a two-dimensional barcode pattern for information management for each chip.

7. *(Previously Presented)* A semiconductor device having at least one semiconductor chip sealed by resin, and having a two-dimensional code pattern for information management provided directly on an outer surface of said resin and representing product ID information, and said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region.

8. *(Original)* A semiconductor device according to claim 7, wherein:

said product ID information includes additional information corresponding to individual chips that are resin-sealed.

9. *(Previously Presented)* A semiconductor device according to claim 7, wherein:

said product ID information corresponds to chip ID information provided as a two-dimensional barcode pattern for information management for each chip.

10. *(Previously Presented)* A semiconductor device according to claim 7, wherein:

said product ID information corresponds to frame ID information provided as a two-dimensional barcode pattern for information management on a lead frame to which semiconductor chips are bonded.

11. *(Previously Presented)* An information management system for semiconductor devices, having at least one semiconductor chip that implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads chip ID information, said chip ID information is provided

directly on a surface of said semiconductor chip by projection and exposure as a two-dimensional barcode pattern for information management for each chip, said two-dimensional barcode pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said chip ID information thus read and manages individual semiconductor manufacturing processes based upon said chip ID information thus registered.

12. *(Previously Presented)* An information management system for semiconductor devices according to claim 11, wherein:

said chip ID information is made to correspond to mapping data obtained during a probing process.

13. *(Original)* An information management system for semiconductor devices according to claim 11, wherein:

said chip ID *information* is projected and exposed using a liquid crystal mask that is capable of changing a light transmitting pattern for each exposure.

14. *(Previously Presented)* An information management system for semiconductor device manufactured using a lead frame, which system implements management of information

related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads frame ID information, said frame ID information is provided directly on a peripheral surface of said lead frame as a two-dimensional code pattern for information management, said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said frame ID information thus read and manages individual semiconductor manufacturing processes based upon said frame ID information thus registered.

15. *(Previously Presented)* An information management system for semiconductor devices according to claim 14, wherein:

said frame ID information corresponds to chip ID information provided as a two-dimensional barcode pattern for information management for each chip.

16. *(Previously Presented)* An information management system for semiconductor devices having semiconductor chips sealed by resin, which system implements management of information related to said semiconductor devices separately for individual semiconductor devices comprising:

a read device that reads product ID information, said product ID information is

provided as a two-dimensional code pattern for information management directly on an outer surface of said resin, said two-dimensional code pattern is comprised of a plurality of square blocks arranged in a matrix in a predetermined two-dimensional region; and

a management unit that registers said product ID information and manages a product shipping process based upon said product ID information thus registered.

17. *(Previously Presented)* An information management system for semiconductor devices according to claim 16, wherein: said product ID information corresponds to chip ID information provided as a two-dimensional barcode pattern for information management for each chip.

18. *(Previously Presented)* A semiconductor device according to claim 16, wherein: said product ID information corresponds to frame ID information provided as a two-dimensional barcode pattern for information management on a lead frame to which semiconductor chips are bonded.

19. *(Previously Presented)* An information management system for semiconductor devices according to claim 16, wherein:

said product ID information that is registered corresponds to manufacturing

process history information corresponding to each chip.

20. *(Previously Presented)* An information management system for semiconductor devices according to claim 16, wherein:

said product ID information that is registered corresponds to claim information regarding claims made in the field after product shipment.

21. *(Previously Presented)* A semiconductor device according to claim 1, wherein said two-dimensional code pattern is formed on said semiconductor chip by photolithography.

22. *(Previously Presented)* A semiconductor device according to claim 7, wherein the blocks of two-dimensional code are formed by laser printing directly on the outer surface of the resin.